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2019

Design, analysis, and comparison of buffers for online multipoint monitoring

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Iowa State University

Design, analysis, and comparison of buffers for online multipoint monitoring

by

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A thesis submitted to the graduate faculty

in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Major: Electrical Engineering (Very Large Scale Integration)

Program of Study Committee:
Degang Chen, Major Professor
Chris Chu
Jiming Song

The student author, whose presentation of the scholarship herein was approved by the program of study committee, is solely responsible for the content of this thesis. The Graduate College will ensure this thesis is globally accessible and will not permit alterations after a degree is conferred.

Iowa State University

Ames, Iowa

2019

DEDICATION

To my family and my friends who have helped me to go through my college careers.

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ACKNOWLEDGMENTS

Dr. Degang Chen *Professor of Electrical and Computer Engineering*

For giving me guidance, explaining my questions, and supporting me with his knowledge

and help to me throughout my master's program, and for serving as my major professor.

Dr. Chris Chu *Professor of Electrical and Computer Engineering*

For serving as my thesis committee member.

Dr. Jiming Song *Professor of Electrical and Computer Engineering*

For serving as my thesis committee member.

ABSTRACT

The increasing complexity of the System-on-Chips (SoCs) used in mission-critical systems such as autonomous cars or planes has led to the need for and various developments of online testing and monitoring methods to monitor circuit functionality and performance of these SoCs. However, the insertion of these monitoring circuits, especially when they are non-ideal, can negatively impact the normal operation or even the basic function of the original circuits. For example, glitches generated by clocks or switches in the monitoring circuits can be coupled into the nodes under test (NUTs) through parasitic capacitors in the original circuits.

To reduce the negative impact on the normal operation, the widely accepted method is inserting analog buffers between the NUTs and the monitoring circuits. For example, a well-designed analog buffer can dramatically reduce the glitch magnitudes coupled to the NUTs by as much as 95%. This thesis will start with systematical analysis on six widely used analog buffers, namely, two Super Source Followers (SSF), two Flipped Voltage Followers (FVF), and 5-Transistor and 7-Transistor buffers. Following that, strategies of optimizing reverse isolation (reverse gain) of these buffers will be derived to enable further reductions of the negative impact of the monitoring circuits. Furthermore, the buffers will be designed and simulated with GF130nm process, and the performance results, such as gain, linearity, reverse gain, etc. will be summarized in a comparison table for easy access. Finally, recommendations of buffers to be used for different applications will be provided.

CHAPTER 1.   INTRODUCTION

1.1 Overview

Monitoring circuits play an important role in System-on-Chips (SoCs), and with the aid of such circuits, engineers can gather critical information that is needed to evaluate system performance or diagnose bugs that may inhibit in the normal operation of the circuits that are being monitored. The first chapter of this thesis is a review of literature about various monitoring circuit architectures, including the introduction of monitoring circuits, and discussion of simulation or measurement results that can demonstrate the convenience and usability of monitoring circuits. One monitoring architecture, Concurrent Sampling (CS) [1], will be discussed in detail, after which the connection between CS and analog buffers will be established.

The second chapter discusses basic buffer topologies in terms of the input range, forward gain, and output impedance, while the third chapter discusses buffer biasing and sizing strategies. The fourth chapter discusses strategies for optimizing buffer reverse gain and compares buffer simulation results. The fifth chapter describes the conclusion of the study.

1.2 Literature Review

There are many papers dealing with circuits or system monitoring. One such paper [2], describes a full monitoring system, called a Signal Integrity Self-Test (SIST) system, for measuring phenomena such as cross-talk, supply noise, substrate noise, temperature, etc.. As shown in Figure 1, different monitoring circuits can be controlled by the SIST controller in

different functional blocks, with measuring circuits converting measured analog signals into digital form and transferred back to the SIST controller for further signal processing.
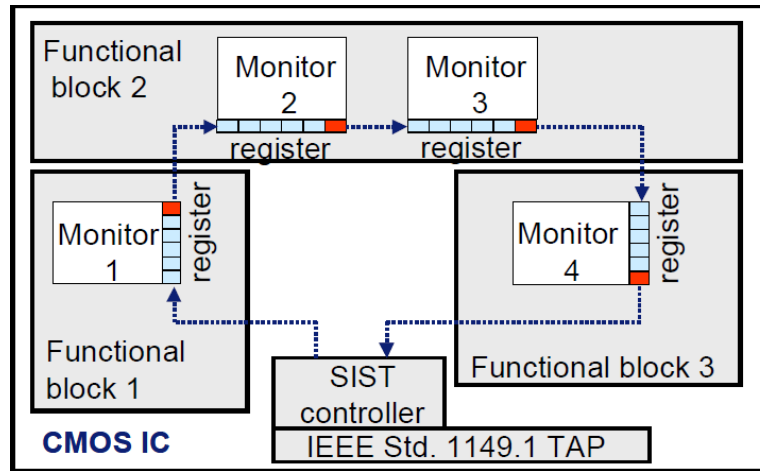
Figure 1 Architecture of a signal integrity self-test system [2].

As shown in Figure 2 below, one of the monitoring circuits – a voltage monitor – is used to monitor a power rail's spikes and dips as a function of system activities. Different Nodes Under Test (NUTs) are connected to the selector and the selector is connected to the comparator, where a DAC provides a reference voltage for use by a comparator to perform a comparison, with the resulting digital results stored in registers for further processing. Results of using voltage monitoring circuits are shown in Figure 3 and Figure 4; such data is very useful in determining a system's power-rail working conditions.
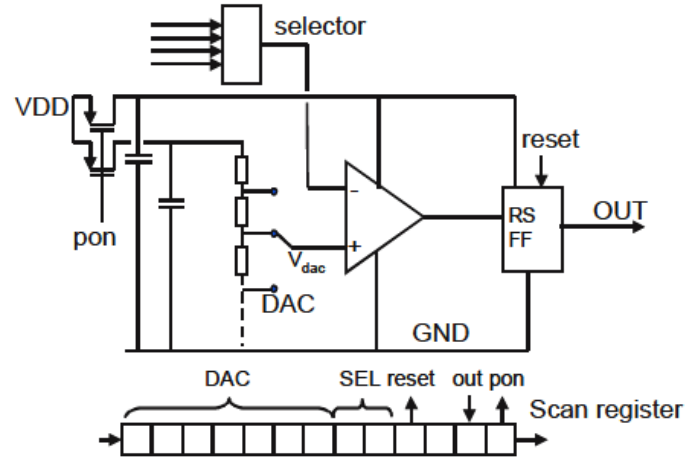
Figure 2 Voltage monitor [1].
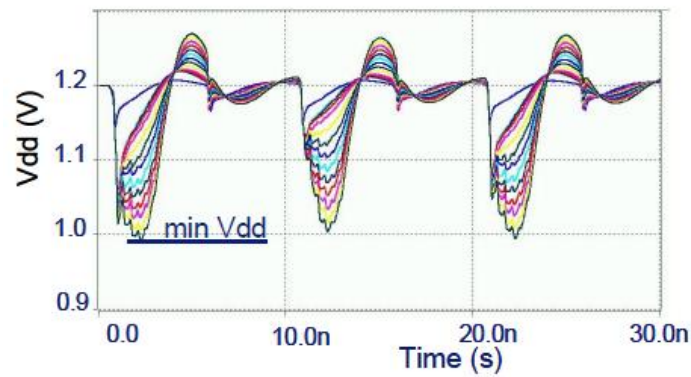
Figure 3 Simulated power rail performance vs. system activities [1].
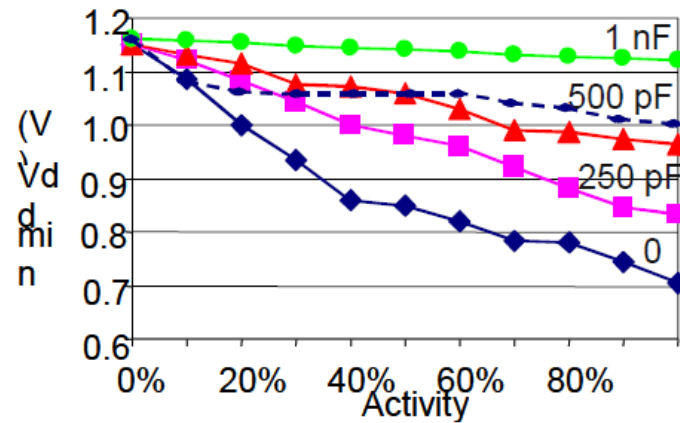
Figure 4 Measured minimum power rail voltage vs. system activities with different decoupling cap [1].

Another monitoring circuit, shown in Figure 5, measures chip temperature, and since it is a bandgap-based structure, the monitor itself can generate a temperature-independent reference voltage.
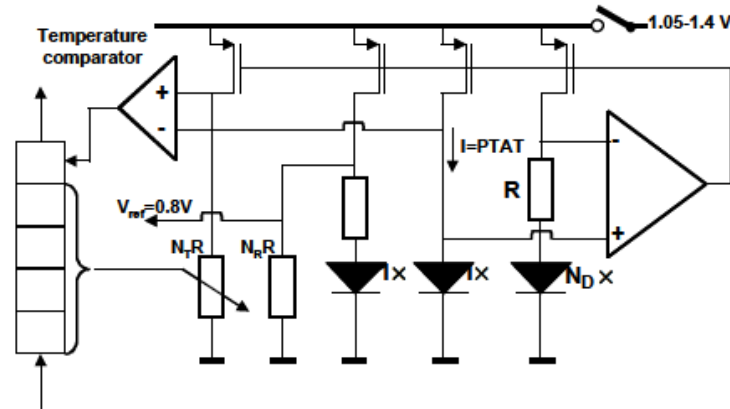
Figure 5 Temperature monitor [1].

Another example of a monitoring circuit is the Analog Test Bus (ATB) [3] whose architecture is shown in Figure 6. The basic operation principle of this architecture is that it contains two global wires – one carrying an analog voltage to the input of an Analog-to-Digital Converter (ADC) and the other one connecting to the ADC's ground reference. The ADC will convert an analog signal into a digital signal, and then it will be further processed by a digital processor.
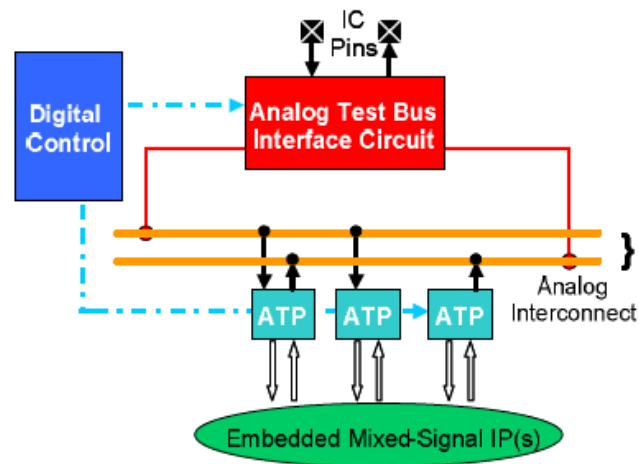
Figure 6 Analog Test Bus (ATB) architecture [3].

There are several drawbacks using an ATB. First, each ATB/ADC pair can measure only one node voltage at a time; if a simultaneous measurement of voltages at multiple nodes is required, multiple pairs must be provided. Second, if multiple nodes are connected to the ATB with switches, then there can be a significant amount of capacitive coupling to the ATB, resulting in a long settling time that will extend the testing time. To overcome ATB drawbacks, a concurrent sampling (CS) method has been developed [1], using the architecture shown in Figure 7.
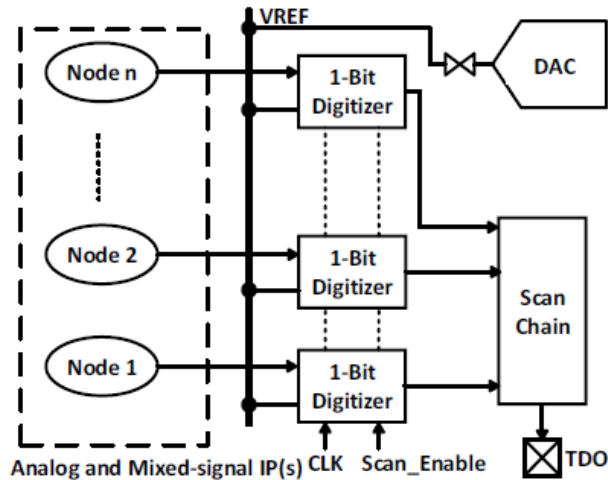
Figure 7 Architecture of the concurrent sampling method [1].

The concurrent sampling method is used to measure DC voltages, and the operation of the CS architecture is similar to the voltage monitor in Figure 2, except that CS can measure several node voltages simultaneously. In operation of the CS, each NUT is connected to a 1-Bit digitizer, i.e., a comparator and a digital-to-analog converter (DAC) whose reference voltage is swept from 0 volts to VDD. Alternatively, many nodes can be connected to switches and share the same comparator, as in Figure 2.

The digitizer will convert the analog signal to digital form with results stored in registers or read out through scan chains. The advantages of using the CS are that it eliminates cross-

coupling between different NUTs, and testing time is reduced since all the nodes can be simultaneously tested.

There is still an issue using the CS method, i.e., noise can be coupled either from the comparator or the switches onto the NUTs. The issue is illustrated in Figure 8, where (1) shows a node is connected to a comparator, and noise, called kickback noise, is generated because of the fast switching of the clock signal coupled from the comparator output back to the input through a parasitic capacitor, as shown in (3). (2) shows that, because of clock feedthrough, noise is coupled from the gate of the switch onto other nodes through parasitic capacitors.
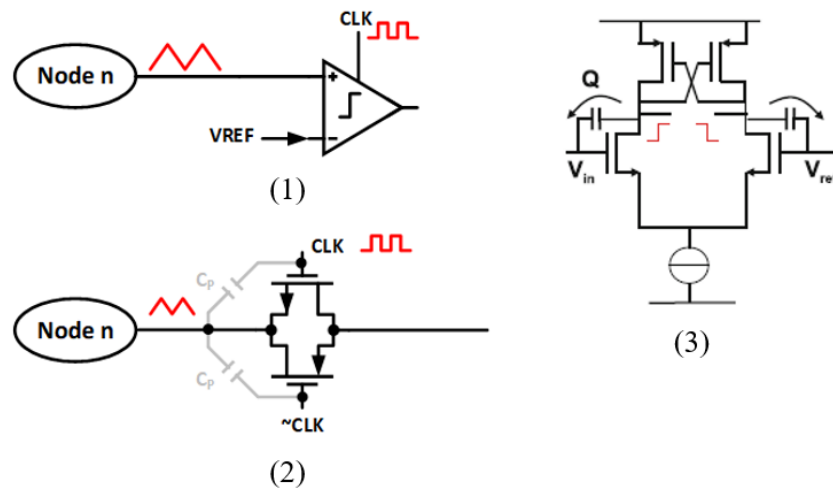
Figure 8 (1) Kickback noise from the comparator to the nodes; (2) Clock feedthrough from the switch to the nodes; (3) Comparator schematic.

One popular approach for reducing such coupled noises is to insert analog buffers between the nodes and the switches or the comparator. Such buffers, commonly used in analog circuits, transform a high input impedance into a low output impedance to reduce loading effects, and can also be used as drivers to drive the following stages of a circuit.

Many studies have been conducted on developing analog buffers, and one of the early examples used a single-stage op-amp as a buffer [4]. As shown in Figure 9, the top four transistors M 4, 5, 7, 8 form a cascode current mirror; at low frequency, the cascode structure

improves the current mismatch issue and increases the DC gain. Two capacitors, C_X and C_C, are used to improve the high-frequency performance, i.e., to extend the buffer bandwidth. Since such a buffer is used for high-frequency applications, some of the frequency-related metrics are gain vs. frequency and harmonic distortion. The plot of Figure 10 describes the forward gain at the DC level, which should be as close as possible to 0dB, and it also shows the locations of 3dB corner frequency for different load capacitors. Harmonic distortion is another important concern in this application, and some typical measurement results are shown in Figure 11.
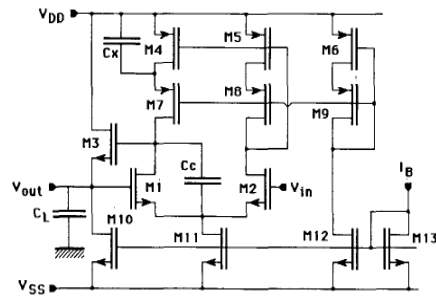
Figure 9 High-frequency buffer schematic [4].
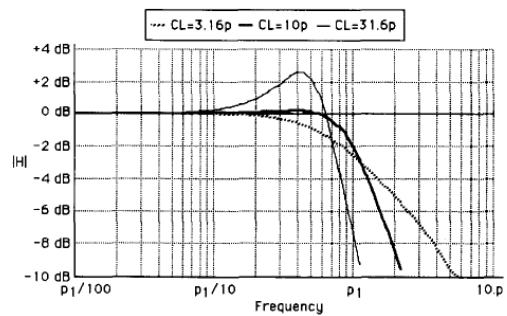
Figure 10 Gain vs. frequency plot [4].
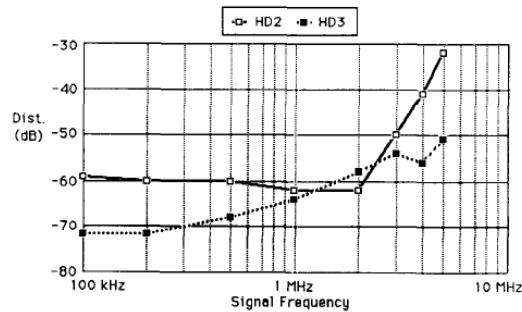
Figure 11 Measured second and third harmonic distortion components of the buffer [4].

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Another op-amp-based buffer example focuses on reducing a buffer's input-output offset and gain error [5] by using a normal 5-transistor based amplifier and connecting a source follower to it to cancel the output offset voltage.

A flipped-voltage-follower (FVF) buffer is another commonly-used buffer topology [6]–[10], offering very low static power consumption, broad bandwidth, very low output impedance, and design simplicity; the drawback of this topology is that its input range is limited by process technology V_{TH} that it doesn't relate to VDD. Flipped-voltage followers are frequently used in applications like a Low Dropout Regulator (LDO) [11]–[14]. In such cases, FVFs are used to drive the gate of the power FET of the LDO, as shown in Figure 12. This approach pushes the low-frequency pole at the gate of the power FET to a higher frequency while simultaneously improves its driving capability and its Phase Margin [15, p. 36]. As shown in Figure 12, after the buffer is inserted, the low-frequency pole at the power FET's gate is transformed into two high-frequency poles.

Analog buffers are widely applied as circuit blocks in the analog-circuit design, and they will be discussed in more detail in the next chapter.
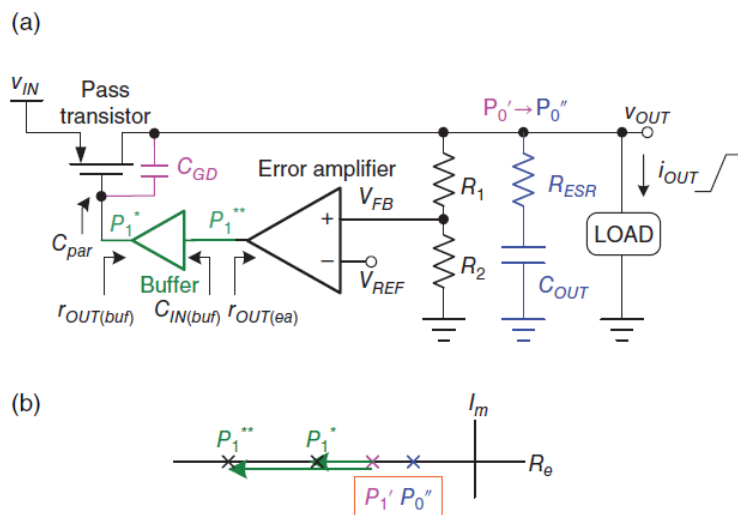
Figure 12 Basic LDO regulator with a buffer stage. (a) Schematic. (b) Root locus [15, p. 36]

CHAPTER 2.   BUFFER TOPOLOGIES REVIEW

2.1 Source Follower

Source follower (also called "common drain") is the simplest buffer which only consists one MOSFET as shown in Figure 13. It senses the input signal at the gate while presenting a high input impedance and drives the load at the source. Depending on whether if it is an NMOS or PMOS input, the output follows the input with a stepped down or stepped up voltage equals to V_{GS}.
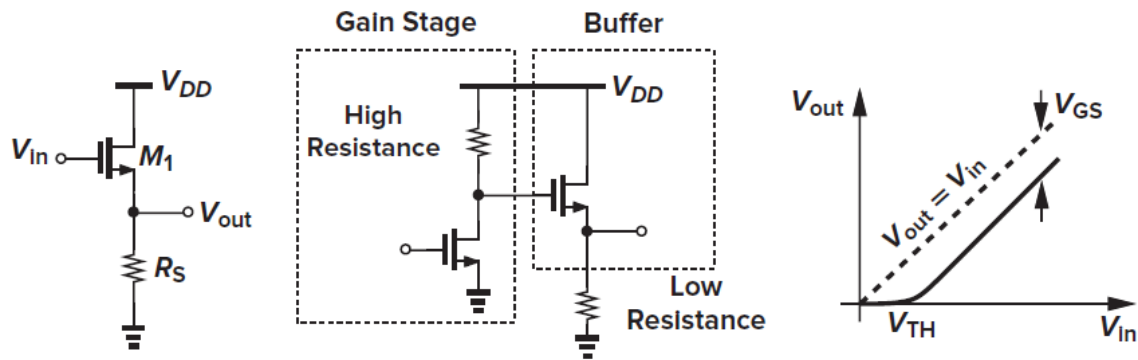
Figure 13 (a) Source follower, (b) example of its role as a buffer, and (c) its input-out characteristic.

In Figure 13 (b) is an example of using Source Follower as a buffer to drive the low resistance load without degrading the voltage gain of the Common Source stage (Gain Stage). Figure 13 (c) is the large-signal behavior of the source follower. For $V_{in} < V_{th}$, M_1 is off and $V_{out} = 0$. As V_{in} researches V_{th}, M_1 starts to turn on and sinks current to R_S. As V_{in} goes further, $V_{out} = V_{in} - V_{GS}$.

One of the characteristics of the buffer we care about is its voltage gain. To get that, first, draw the small-signal circuit of the source follower circuit as shown in Figure 14. By inspecting the circuit, we have $V_{in} - V_{out} = V_1$, $V_{bs} = -V_{out}$, and $g_m V_1 + g_{mb} V_{bs} = V_{out}/R_s$. Thus, the voltage gain becomes

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_m R_S}{1+(g_m+g_{mb})R_S}. \tag{1}$$
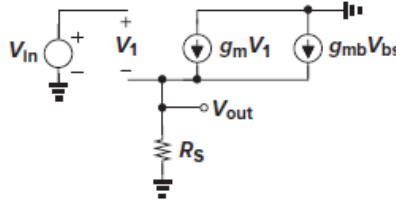
Figure 14 Small-signal equivalent circuit of the source follower.

The output impedance is another characteristic we care about while designing a source follower buffer. It can be calculated with the aid of a small-signal circuit shown in Figure 15. Note the channel length modulation is neglected in this case. We write $V_{bs} = -V_X, -g_m V_X - g_{mb} V_X = -I_X$. So, the output impedance

$$R_{out} = \frac{1}{g_m + g_{mb} + 1/r_0 + 1/R_L} \tag{2}$$

This output resistance is about a few kΩ.
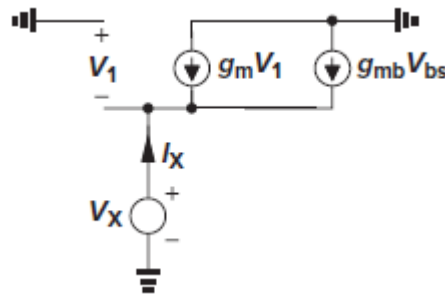
Figure 15 Source follower output impedance calculation.

Because the drain current depends heavily on the input level, so the source resistor is replaced by a FET which provides constant current biasing for the input FET as it is shown in Figure 16. And the small-signal gain becomes

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_m(r_{ds1}||r_{ds2})}{1 + (g_m + g_{mb})(r_{ds1}||r_{ds2})}. \tag{3}$$
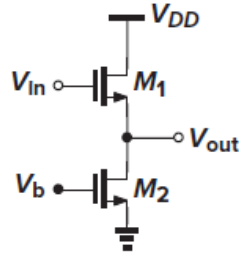
Figure 16 NMOS used as a current source.

The gain of the source follower will be close to unity, but it will never reach unity because the change of the input level will lead to the change of the threshold voltage Vth, and this will reduce the gain and introduce non-linearity on the source follower. Let us look at this in an example, with the help of two equations and circuit in Figure 16

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{th})^2, \tag{4}$$

$$V_{th} = V_{TH0} + \gamma(\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}). \tag{5}$$

Without body effect, i.e. V_{th} does not change. If V_X decreases by ΔV, V_{GS} increases by ΔV and current increases. However, if body effect is included, with V_X decreases by ΔV, V_{th} will decrease as well based on (5). So then, in (4) we have V_{GS} term increases and V_{th} term decreases, the current experiences a greater change and hence a lower output impedance.

Overall, the source follower has a high input impedance and a moderate output impedance. But it has nonlinearity due to body effect and voltage headroom consumption due to level shift.

2.2 Super Source Follower

In terms of transient response, the PMOS super source follower in Figure 17 has stronger current sinking ability than sourcing ability. The current sourcing ability is limited by the total current I3 provided by M3, and most of I3 will flow into M4 and M2, so the current left for charging the output node is I$_{source}$= I3 – I4 – I2. But the PMOS SSF has a strong current sinking

ability, during the down slew of the transient response, the transient current I$_{tran}$ at the output capacitor will be discharged into the output node, so the sinking current I$_{sink}$ =I3 + I$_{tran}$. If the SSF is built into NMOS version, then it will have strong sourcing capability but limited sinking ability.

The input range is another spec we care about, for the PMOS SSF the input range is $V_{GS2} - V_{TH1} < V_{IN_{PSSF}} < V_{DD} - V_{DSsat3} - V_{GS1}$, this is approximately $V_{DSsat} < V_{IN_{PSSF}} < V_{DD} - 2V_{DSsat} - V_{TH}$. The SSF can also be used as a voltage level shifter due to the $+|V_{GS1}|$ or $-|V_{GS1}|$ shift from input to output for PMOS and NMOS version.

In terms of small-signal gain and output resistance, as we saw in the previous section that a source follower's output impedance is $1/g_m + g_{mb}$. For some low resistance load, this output impedance may not be low enough which will cause the loading effect on the output of the buffer. One way to reduce the output impedance is to increase the FET's g_m which can be done through increasing FET size or increasing biasing current. But this approach will require a proportionate increase in the layout area and power consumption. An alternative way to increase the output impedance without increasing much area or power is using Super Source Follower (SSF) as shown in Fig. 5. The circuit uses M2 to reduce the output impedance through negative feedback. Suppose V_{out} increases and V_{in} stays constant, then V_{GS1} increases and leads to M1 drain current increases, and this increase V_{GS2}. As a result, I_{D2} increases, reducing the total output impedance by increasing the total current that flows into the output node.
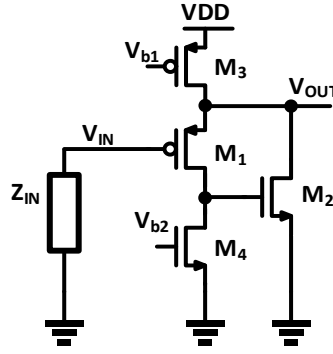
Figure 17 PMOS super source follower.

With the help of small-signal analysis, the R_o of the SSF can be found as:

$$R_o \cong \frac{1}{g_{m1} + g_{mb1}} \left(\frac{1}{g_{m2}r_{01}}\right) \tag{6}$$

If we compare the Equation (2) and (6), we can see the output resistance is reduced roughly by a factor of $g_{m2}r_{01}$. The open-circuit voltage gain of SSF is

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{1}{g_{m2}r_{02}}} \tag{7}$$

Comparing the gain of a source follower and SSF with equations (1) and (7), if $g_{m2}r_{02} \gg 1$, then their gain is close. If the $g_{m2}r_{02}$ term is not much bigger than 1, then SSF's gain deviates more from the unity gain than a source follower.

2.3 Flipped -Voltage Follower

The flipped – voltage follower (FVF) was invented based on the source follower to address the problem of high output impedance and signal-dependent biasing current. The FVF from Figure 18 has an output impedance $R_o = 1/(g_{m1}g_{m2}r_{o1})$ which is around tens of Ωs, and high current-sinking capability, and low supply requirement $V_{DSsat} + V_{GS2}$ which is close to a FET's V_{TH}. The M2 is used as shunt feedback to reduce the output current variation. Suppose

V_{out} increases, which increases the V_{GS1} and this increase the I_1. As I_1 increases, V_{FB} will be increased which in turn decreases the V_{GS2} and decreases the I_2.
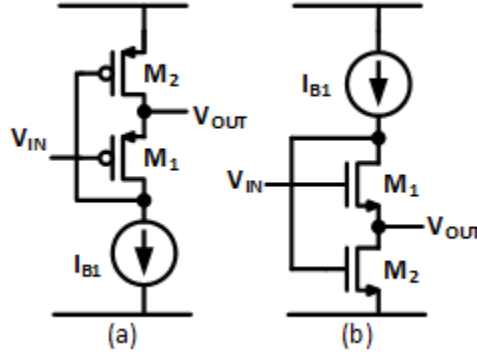
Figure 18 Flipped voltage follower (a) PFVF; (b) NFVF

The disadvantage of using FVF is its limited input and output range. The input range for the FVF is $VDD - V_{GS2} - V_{TH1} < V_{IN} < VDD - V_{DSsat2} - V_{GS1}$ which is about a V_{TH} and this range does not depend on the VDD level but depends on the V_{TH}. In a smaller node technology, the V_{TH} will be further decreased from .4V as in .13um process which limits the use of FVF. The forward gain for the FVF is listed below, and g_{ds3} is the current mirror's r_{ds}.

$$A_V = \frac{V_{out}}{V_{in}}$$
$$= \frac{g_{m1}g_{m2} + g_{m1}g_{ds3}}{g_{m1}g_{m2} + g_{ds1}g_{m2} + g_{ds1}g_{ds2} + g_{ds3}(g_{m1} + g_{ds1} + g_{ds2})}$$

(8)

Assume that the current mirror's r_{ds} is infinite, then the forward gain becomes:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{ds2}}$$

(9)

2.4 Op-Amp Based Buffer

Before we start to talk about the op-amp based buffer, we should first review the general

feedback block diagram as shown in Figure 19. "*A*" is the open loop forward gain, and it is

usually 80~90dB, which is hard to control if it is used in the open-loop configuration. A little

disturbance at the input will saturate the output to the power supply level. β is the feedback

factor. The output to the input transfer function of the feedback system is

$$\frac{Y(s)}{X(s)} = \frac{1}{\frac{1}{A} + \beta} \tag{10}$$
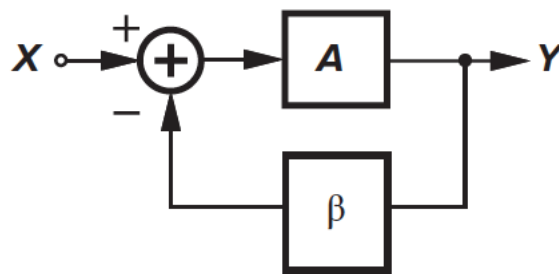
Figure 19 Simple feedback system.

An op-Amp based buffer is a commonly used application in discrete component design,

as well as in integrated circuit level. The basic structure is having an op-amp connected in

negative feedback fashion, and its feedback factor β = 1, as is shown in Figure 20. Assume the

op-amp has 90dB gain, which is around 30,000, the closed-loop gain is 0.99996666777. So, the

higher A is, the closer to 1 for the buffer accuracy.
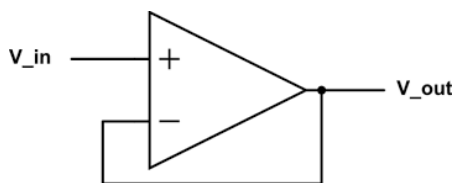
Figure 20 An op-amp based buffer.

The simplest and widely used amplifier topologies are 5 transistors OTA and 7 transistors Two-Stage Op-Amp. The OTA has only 5 transistors, which allows it uses less power (assuming same tail current biasing for the OTA and Two-stage Op-Amp), but its input and output range is not as wide as Two-Stage Op-Amp's. And the Two-Stage Op-Amp has higher open-loop gain, which means output voltage follows input voltage more accurately. An OTA has about 30 dB gain and Two-Stage Op-Amp has 60 dB gain.
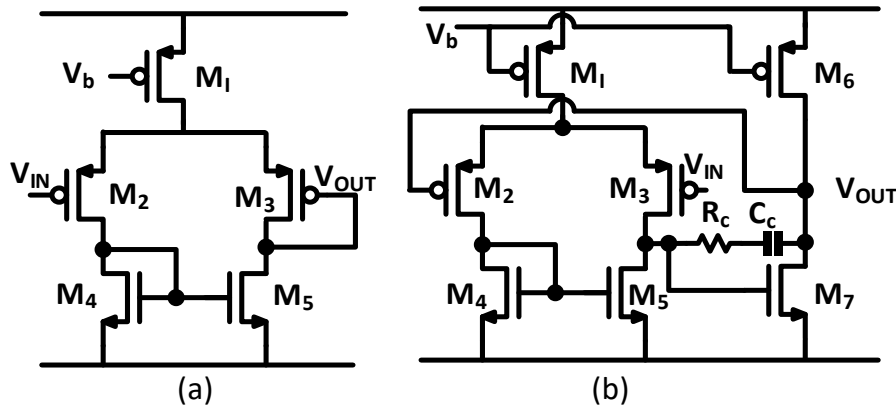
Figure 21 Op-Amp based buffer. (a) OTA buffer (b) Two-stage Op-Amp buffer.

The input ranges for (a) and (b) in Figure 21 are

$$V_{GS4} - V_{TH2} < V_{IN\_OTA} < VDD - V_{DSsat1} - V_{GS2} \tag{11}$$

$$V_{GS4} - V_{TH3} < V_{IN\_OPAMP} < VDD - V_{DSsat1} - V_{GS3} \tag{12}$$

As we can see from the equations above that two buffers have the same input range.

A brief mention of the methodology to calculate the output resistance for a voltage-voltage feedback circuit. As shown in Figure 22, where R$_{out}$ is the output impedance of the feedforward amplifier.
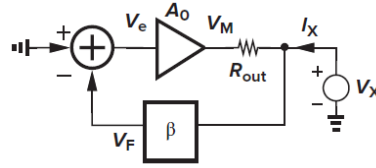
Figure 22 Calculation of output resistance of a voltage- voltage feedback circuit.

Setting the input to zero and applying a voltage at the output, we get an expression

$$\frac{V_X}{I_X} = \frac{R_{out}}{1 + \beta A_0} \tag{13}$$

With the help of the above equation, we can find the output resistance for the OTA and

Op-Amp's output resistance easily, which are $1/g_{m2}$ and $1/g_{m2}r_{o1}g_{m7}$.

One of the applications of the buffers we emphasis in this thesis is the node to node

isolation. As the application is shown in the Concurrent Sampling, the buffers are used to

minimize the glitches that have been generated from the comparator clock signal cross-coupled

on to the Node Under Testing (NUT). The name of this cross-coupling phenomena is called

Clock Feedthrough or Charge Injection. It is the clock signal that connected to the gate of the

FET and got coupled onto the drain or source of the FET through the FET's parasitic caps.
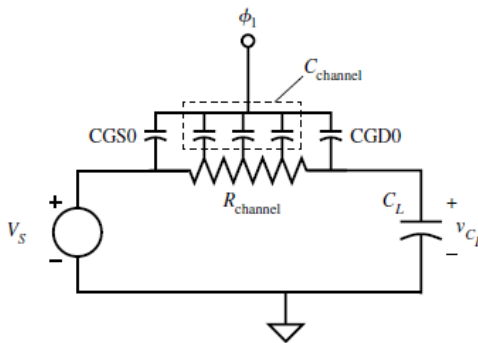
Figure 23 Clock feedthrough model.

As the buffers inserted between the NUTs and the comparators, it provides a reverse gain

which attenuates the coupled clock signals to the NUTs to a very low value, which is essentially

reducing the glitch energy.

CHAPTER 3.   BUFFER BIASING AND SIZING STRATEGIES

3.1 Super Source Follower

As I have briefly touched upon the biasing strategies for the super source follower in Chapter 2, I will talk about that in details in this chapter, about the sizing and biasing strategies. The super source follower circuit in Figure 17 can be biased with a reference current source and current mirrors as shown in Figure 24, and there's no exact guideline about how much current each buffer should use, the rule of thumb is to use as little current as possible, but still maintain the expected performance.
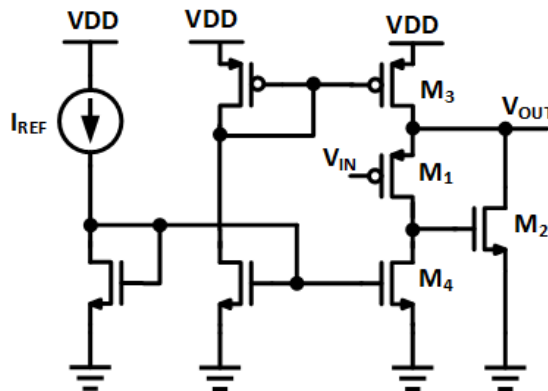
Figure 24 Super source follower with reference current biasing.

The biasing on the buffer will affect many aspects of the circuit performances, like the input range, gain and output impedance. Depending on the application of the buffers, the bias can be optimized towards different perspectives. For example, the buffer can be optimized towards a wider input range, better isolation (reverse gain), better linearity, etc. Based on the MOSFET square law models, for the buffers to have large input range, each FET should be designed in large size, so they will take less voltage headroom which is good for widening the voltage swing range.

While increasing the size for the input FET, it is not only increasing the input range but also increasing the linearity of the SSF. As we can see from the gain equation of the SSF:

$$A = \frac{g_{m1}r_{o1}}{1 + (g_{m1} + g_{mb1})r_{o1} + \frac{1}{g_{m2}r_{02}}} \tag{14}$$

Increasing the M1 size means making the gm1 dominating the gain equation which in return makes the gm2*ro2 term has less weight on the equation, which causes less nonlinearity on the buffer because as gm1 becomes large enough, the gain "A" is becoming very close to 1. And this linearity improvement can be seen in chapter 4 from Table 1.
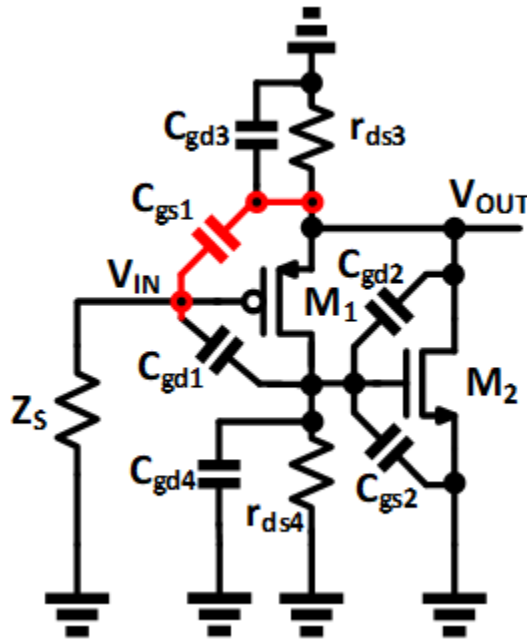
Depending on the application of the buffer, not only the input range and the linearity will be concerned, but also how well that a buffer can suppress the noise from one circuit to another. In this case, a small signal backward gain can be derived for the SSF:

$$A_{ISO} = \frac{V_{IN}(s)}{V_{OUT}(s)} = \frac{s^2 C_{gs1}C_{gs2} + sC_{gd1}g_{ds1}}{s^2 C_{gs2}C_{IN} + sC_{gs2}g_{IN} + 2g_{ds1}g_{IN}} \tag{15}$$

This backward gain describes how the output noise is being attenuated when it's been coupled to the input of the buffer with the transistor parasitic capacitors. And at high frequency, the $A_{Backward}$ becomes $\frac{C_{gs1}}{C_{IN}}$, and the smaller the $A_{Backward}$ is the better. C_{IN} is the overall capacitance from the input device, and C_{gs1} is the parasitic capacitor from the input FET and it relates to the size of the transistor with the equation below

$$C_{gs} = \frac{2}{3}WL_{eff}C_{ox} + WC_{OV} \tag{16}$$

L_{eff} is the effective channel length, C_{ox} is the gate oxide capacitance per unit area and C_{OV} is the overlap capacitance per unit width.

3.2 Flipped Voltage Follower

As it was stated in the previous section that an FVF's input range is limited by the threshold voltage V_{TH} and the V_{TH} is directly dependent on the process technology. And as we examine the gain equation of the FVF from the **Error! Reference source not found.**, we find its g ain is only dependent on the gm*ro, which is called the "intrinsic gain" of a MOSFET, and this quantity represents the maximum voltage gain that can be achieved using a single device. In this case, the FVF's gain is decided by the process technology, the same as its input range. The biasing or sizing strategies will not change the range of the input range or make the gain be more linear, rather, they only shift the range towards either higher or lower voltage input, and this result can be seen in the design example of the FVF.
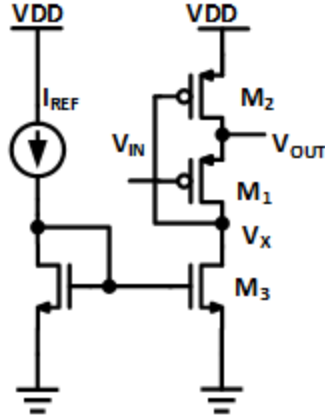
Figure 25 FVF with reference current.

And to find the backward gain, we write the small-signal equals at the V_{OUT} and V_X node:

At the output node:

$$(V_X - V_{OUT})sC_{gd2} - V_{OUT}g_{m2} = (V_{OUT} - V_{IN})(g_{m1} + sC_{gs1}) \qquad (17)$$

At the V_X:

$$-V_X sC_{gs2} + V_{OUT}g_{m1} - V_{IN}(g_{m1} - sC_{gd1}) - V_X sC_{gd1} = V_X g_{ds3} \qquad (18)$$

Equating the two equations together, and get the backward gain, which is:

$$A_{ISO} = \frac{V_{IN}(s)}{V_{OUT}(s)} \approx \frac{C_{gs2}C_{gd2}}{C_{gs1}C_{gs2} + C_{gs1}C_{gd1}} \qquad (19)$$

From the above equation, we can see to design the input FET as small as possible to make the

$A_{Backward}$ as small as possible to attenuate the coupled noise from the output onto the input. And

to understand this conclusion intuitively, the direct coupling between the input and the output is

C_{gs1}, and its impedance is $1/sC_{gs1}$, so the smaller the cap is, the larger the impedance is, which

means noise will be harder to pass from output to input.

3.3 5T Buffer
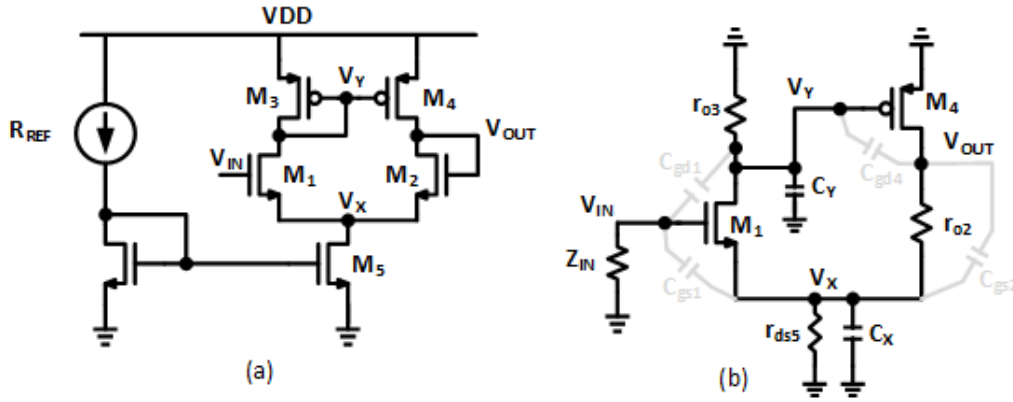
Figure 26 (a) 5T buffer; (b) 5T buffer small-signal diagram.

To analyze the noise coupled from the output node onto the input node and get reduced by the negative feedback from a large signal point of view, assume a rising voltage appeared at the V_{OUT} in (a) of Figure 26, then there will be more current flowing into node V_X from the FET M2 and it charges up the voltage on this node, and in saturation, $V_g = V_{gs} + V_s$, so when the V_X is been charged up, the V_{IN} will be increased to $V_{IN} + V_X$. Then this noise gets amplified by the gain of M1 from V_{IN} to V_Y. When the V_Y is high, it will provide less current from M4 to M2, which in terms reduces the voltage V_{OUT}. To optimize this negative feedback, meaning reduce the noise area on the transient simulation, we can provide the 5T buffer with more tail current. The effect of this can be seen later in the design example section.

To analyze the noise from the small-signal perspective as shown in (b) of Figure 26. The small-signal diagram does not have all the parasitic capacitors shown in the diagram but only shown the caps which contributes the most on the buffer backward gain A_{ISO}. There are two paths that the noise can be coupled from the output of the buffer onto the input, and they are the upper path $V_{OUT} \rightarrow C_{gd4} \rightarrow V_Y \rightarrow C_{gd1} \rightarrow V_{IN}$, and the lower path $V_{OUT} \rightarrow r_{o2} \rightarrow V_X \rightarrow C_{gs1} \rightarrow V_{IN}$. The lower path has the impedance of $1/g_{m2} + 1/sC_{gs1}$, and the upper path has $1/s(C_{gd3} + C_{gd4})$.

Because g_m is usually in the range from 10 to 20 μS, and C_{gs} is much larger than C_{gd} in fF level,

so the lower path has less impedance, which means most of the noise from the output node will

be coupled to the input node through this path. To mathematically prove it, we can write the

KCL equations for the small-signal model.

From V_{OUT} to V_X there is a capacitance divider:

$$V_X = \frac{sC_{gs2} + g_{m2}}{sC_{gs2} + g_{m2} + sC_X + g_{ds5}} V_{OUT} \tag{20}$$

From V_X to V_{IN} is a high pass filter:

$$V_{IN} = \frac{sC_{gs1}}{1 + sC_{gs1}R_{IN}} V_X \tag{21}$$

Combine the above two equations together, the transfer function becomes:

$$(V_{IN} - V_X)g_{m1} + (V_{OUT} - V_X)g_{o2} = V_X Y_X \tag{22}$$

From the three equations above we can get the backward gain as:

$$A_{ISO} = \frac{V_{IN}}{V_{OUT}} = \frac{sC_{gs2} + g_{m2}}{sC_{gs2} + g_{m2} + sC_X + g_{ds5}} * \frac{sC_{gs1}}{1 + sC_{gs1}Z_{IN}} \tag{23}$$

At high frequency, the above equation can be further simplified, the first term

approximately equals to $1/Z_{IN}$; and in the second term, the g_{m2}, and the g_{ds5} term can be

omitted, which leaves only $C_{gs2}/(C_{gs2} + C_X)$ in the second term, and this term is approximately

equal to 1, because C_X is the sum of C_{gd5}, and C_{db5} which are much smaller than C_{gs}.

3.4 7T Buffer
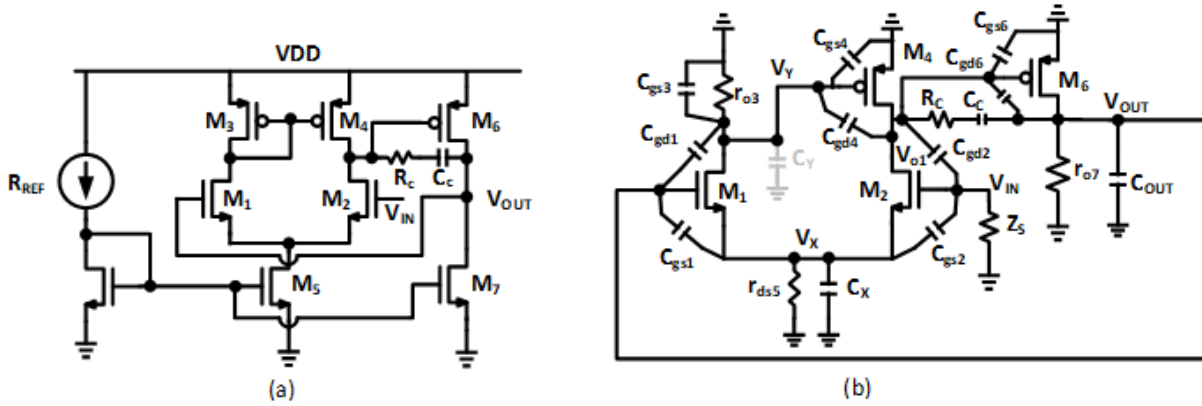
Figure 27 (a) 7T buffer; (b) 7T buffer small-signal diagram.

The analysis for the 7-transistor buffer is similar to the 5-transistor buffer, and because 7T buffer has higher open-loop gain, so inherently, it has better noise isolation performance than the 5T buffer. In Figure 27 (b), there are three paths that the output noise can be coupled onto the input node – V_{OUT} -> C_{gd6} -> C_{gd2} -> V_{IN}, V_{OUT} -> C_{gs1} -> V_X -> C_{gs2} -> V_{IN}, V_{OUT} -> C_{gd1} -> V_Y -> C_{gd4} -> V_{o1} -> C_{gd2} -> V_{IN}, and the second path is the main path since C_{gs} are much larger than other parasitics, so C_{gs} has less impedance and easier for noises to be traveling through. The transfer function for the 7T buffer from V_{OUT} to V_{IN} can be found as:

$$A_{ISO} = \frac{V_{IN}}{V_{OUT}} = \frac{C_{gs1}}{C_{gs1} + C_X} * \frac{sC_{gs2}}{1 + sC_{gs2}Z_S} \qquad (24)$$

As we can see there is a capacitive voltage divider from V_{OUT} to V_X first, and then there's a high-pass filter from V_X to V_{IN}. The reverse gain optimization strategy is the same as for 5T buffer – increase the C_X or giving more tail current to boost the open-loop gain of the op-amp which results in faster transient response.

3.5 Buffers Sized for Comparison

The above sizing strategies are for optimizing the individual buffers' forward gain, backward gain (or reverse gain), and input range. However, to compare the performance of the buffers, other sizing and biasing strategies need to be adopted. There are many specs can be fixed to do the performance comparison, the strategy that has been chosen in this case is making all the buffers have the same current, and all the buffer's input FETs are in the same size. The reasoning for fixing all the input FETs in the same size is because as the equations showed, the backward gain is related to the input FETs' sizes, so if they are fixed to the same, the different of the backward gain between different buffers are caused by topology differences.

The minimum current needed for each buffer is decided by the total current that is been used for the 7 MOS buffer, in this case, it's 35uA. For the FVF, M1 and M2 will have the same current, because those two FETs are in the same branch. For the SSF, M1 will have the most current, about 30uA, and M2 will take 5uA current, because the larger the current is, the larger the gm will be, and large gm1 will help to make the forward gain closer to 1. For the 5 MOS, the 35uA current will be split evenly between M1 and M2. For the 7 MOS, the second stage will take 30uA current and the first stage will take 5uA and split equally between M1 and M2.

CHAPTER 4. BUFFER DESIGN AND SIMULATION

4.1 SSF

A. Input range and linearity Optimization

The SSF in Figure 28 is being biased by a 5uA current source, and the VDD is 1.5V, the input voltage is designed with .8V as input common-mode voltage.

As it was mentioned in chapter 3, to have a wide input range the FETs should be designed to bigger size to minimize their voltage headroom. So, in the example below, the input FET's size is being increased with its multiplier and the input range is also being increased as it is shown in Figure 29.
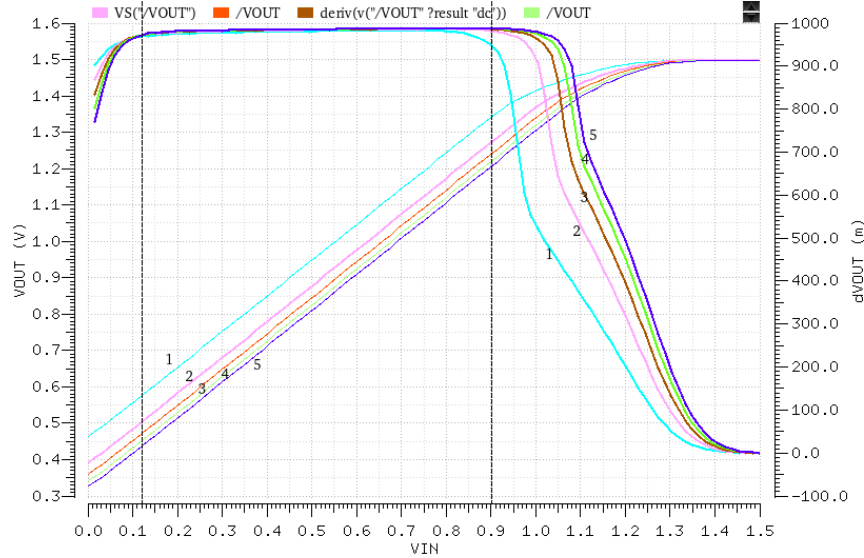

Figure 28 SSF cadence schematic.

Figure 29 SSF Vin vs. Vout and Vout derivative.

Figure 29 is the simulated Vin vs. Vout and Vout's derivative with the different sizes of the input FET. The size was increased by changing the multiplier from 1 to 5 with fixed width and length on the input FET, and the Vout is exported and calculated into the number of bits in the MATLAB. To do that, the input voltage was first swept from 0 to 1.5V as shown in Figure 29, take the Vout signal and select a range that all transistors are in saturation region, in this case, from 0.2 to 0.9V, and then using the MATLAB to calculate the INL and convert it to the Number of Bits. (The MATLAB codes will be included in the appendix)

Table 1 FET size vs. Linearity.

Multiplier	1	2	3	4	5
# of Bits	9.68	9.85	9.99	10.07	10.11

As we can see from Table 1 FET size vs. Linearity. Table 1 that increasing the input FET's size can improve the buffer linearity. That is because increasing the size will increase the $gm1$, and based on the small-signal gain equation, as $gm1$ increases, the nonlinearity due to $gm2$ will have less effect, so the linearity improves.
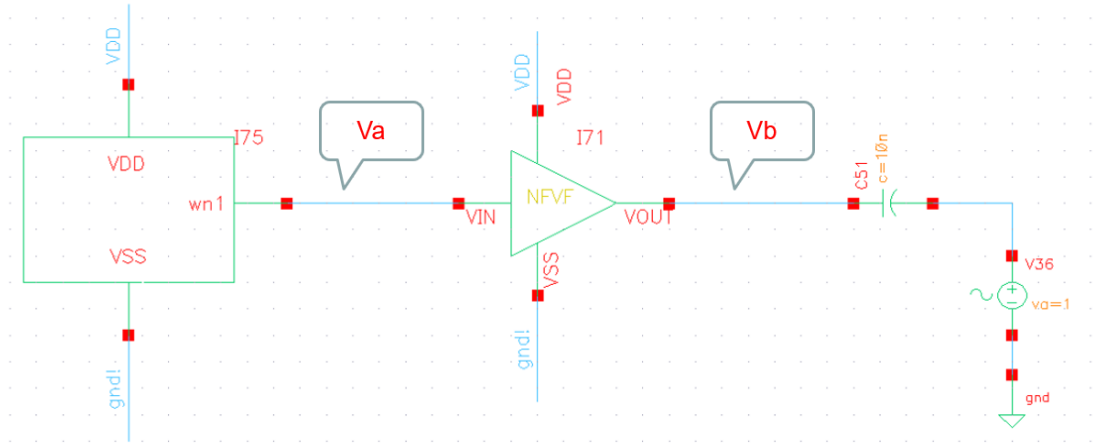
B. Isolation Optimization
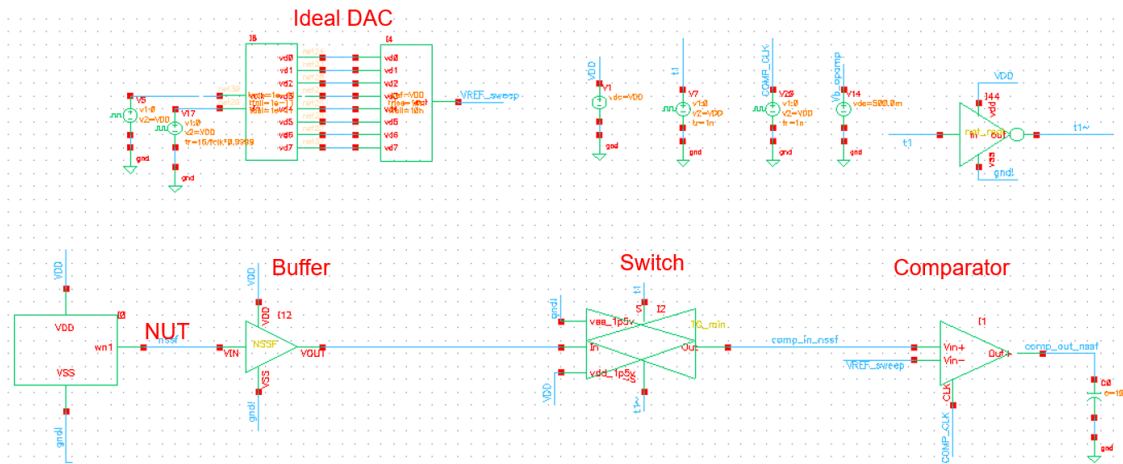

Figure 30 Buffer AC test testbench.

Figure 31 Buffer transient test testbench.
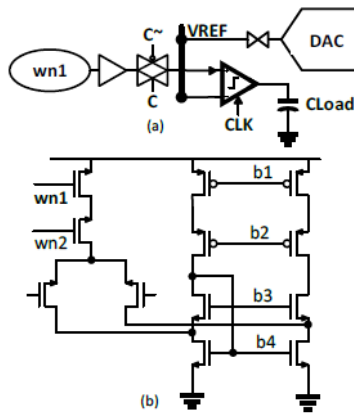
Figure 32 (a) Isolation test bench; (b) Device under test.

The test bench for testing the buffer isolation is as shown in Figure 30 and Figure 31. The Node of Testing (NUT) is an analog voltage node from an Op-Amp's tail current biasing node. It is connected to a buffer and the buffer is connected to a transmission gate and the transmission gate is connected to a comparator. A DAC is used to generate the VREF sweep and it is been fed into the comparator. The digital switching noise will be coming from the transmission gate's and comparator's clock, as when the clock switches from VSS to VDD, the charge injection and clock feedthrough introduces the noise on the NUT.

Figure 33 Buffer AC performance with different input FET size.
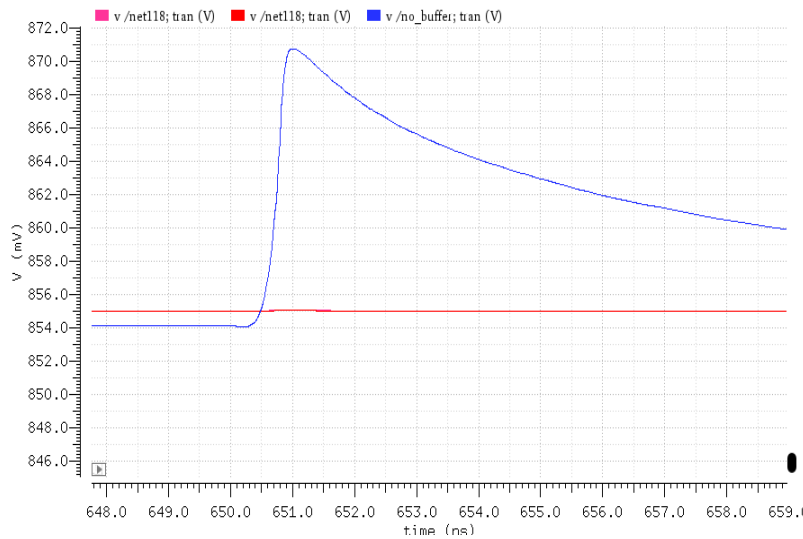
Figure 34 Isolation of no buffer vs. with buffer.

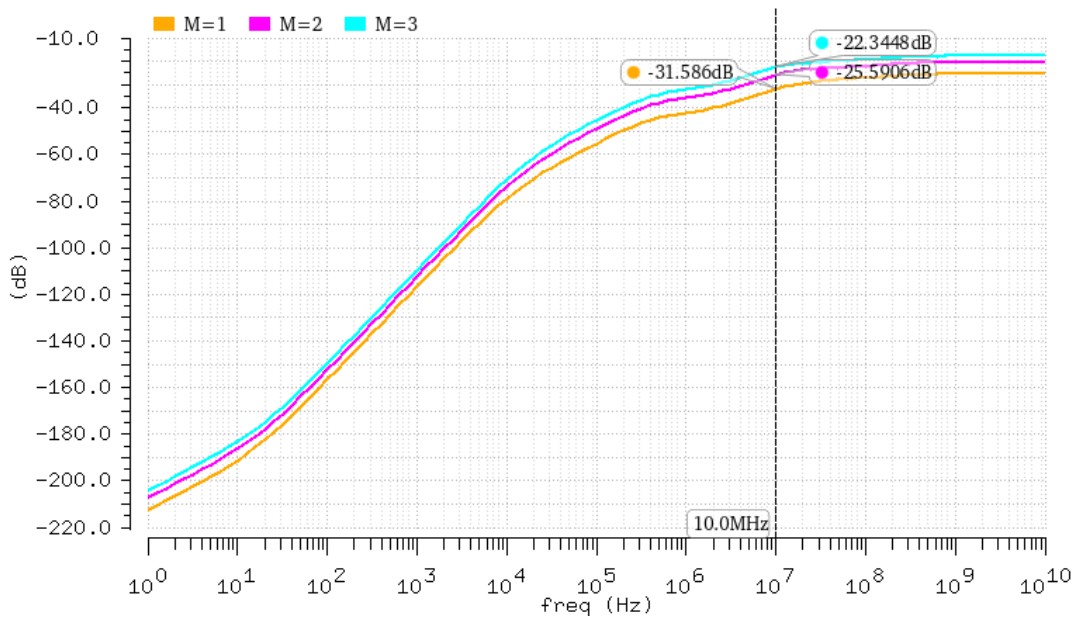As we can see from Figure 34, the blue line is without a buffer used in the circuit, and the red and pink lines are with a buffer used. There's a big difference whether if a buffer used, as it can reduce the glitch noise tremendously – with a reduction on the glitch noise of 95% from 40 nsV to 2nsV, which in term protects the DC biasing point of the NUT.
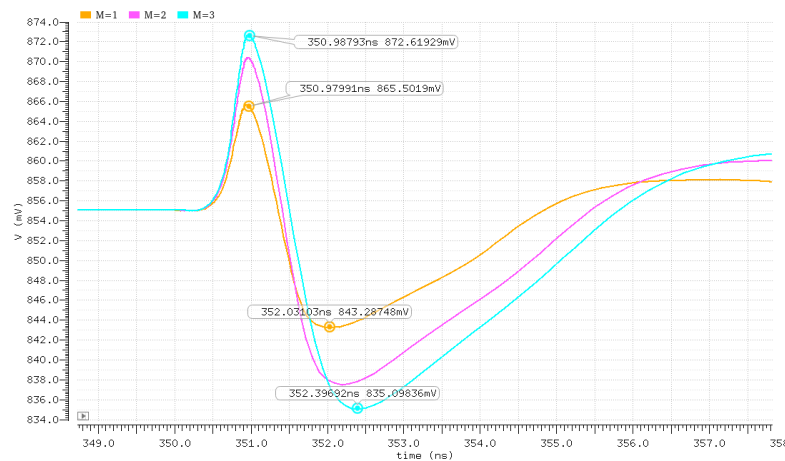
Figure 35 Transient simulation of isolation vs. input FET size.

As we got the result from the design strategy section that smaller input FET size leads to a better isolation performance, and this is shown in Figure 35. The pink line represents the buffer with the biggest input FET size and the blue line represents the buffer with the smallest input FET size, and it is very obvious that the smaller the size is, the smaller the glitch will be.

4.2 FVF

A. Input range and linearity
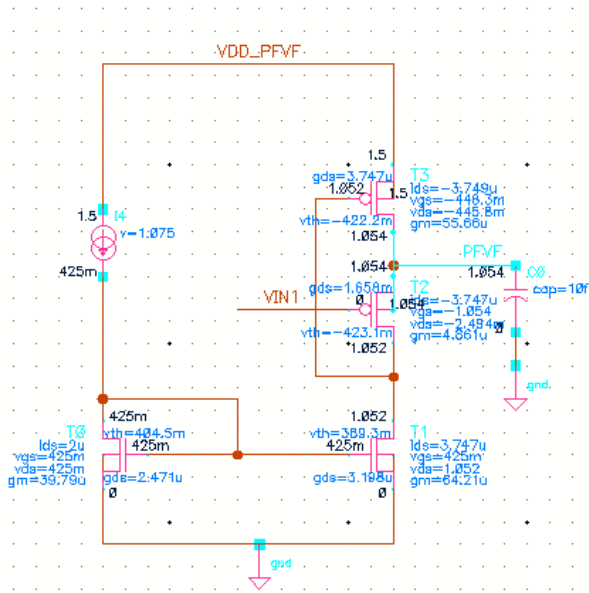
Figure 36 FVF cadence schematic.
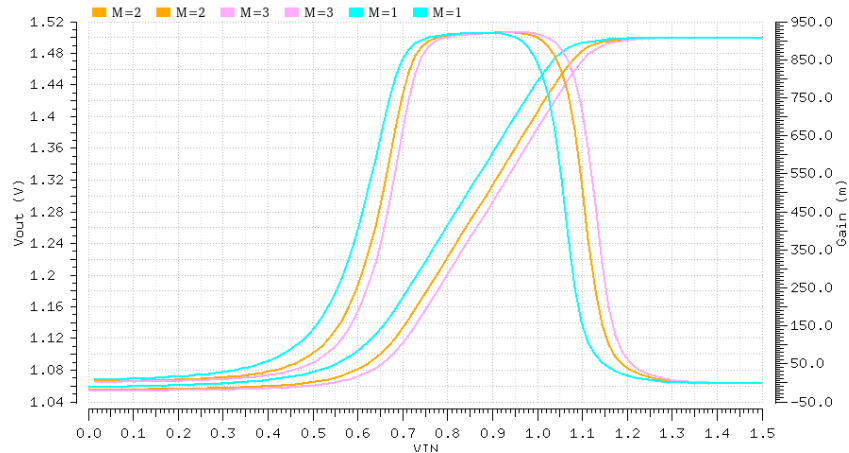
Figure 37 FVF size vs. Vout and Vout derivative.

Table 2 FVF linearity vs. FET size.

	M=1	M=2	M=3
# of Bits	9.1	9.52	8.94

In Figure 37, buffers with input multiplier changed from 1 to 3, and their Vin vs Vout and Vin vs. derivative Vout are plotted. From the plot, we can see the input range did not become obviously bigger when the input FET's size increases, it's rather just shifted towards bigger input

level. And from Table 2, we can see the linearity first increases slightly with the size increases, and then it decreased once the size is bigger. This is close to the analytical result which says there is a limit for the linearity performance. The reason that the linearity is improving, in this case, is that there are some assumptions and approximations used during the analysis. In the analysis, we assumed M2 does not change the linearity performance of the buffer, but in reality, it still does, so the discrepancy between the equation and the simulation. And what happened at M=3 is the upper pFET went into triode region, which caused the drop of the linearity.

B. Isolation Optimization

Figure 38 FVF undershoot glitch.
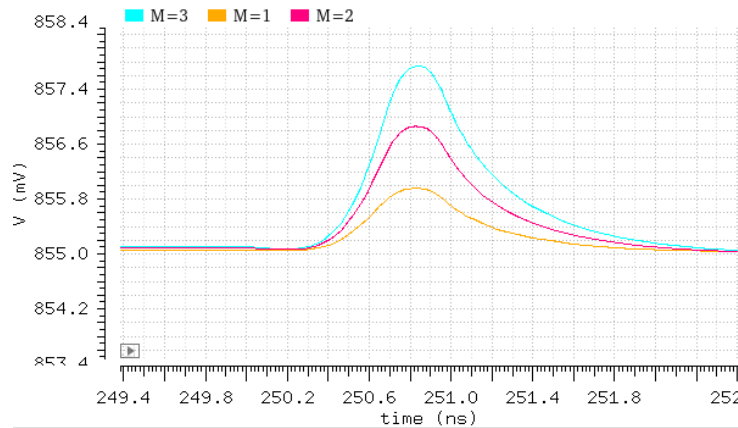
Figure 39 FVF overshoot glitch.

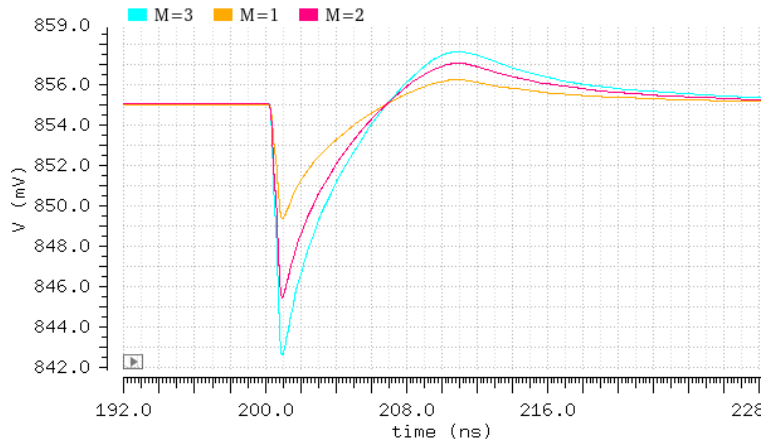From the plots in Figure 38 and Figure 39 we can see that the smaller the input FET size is, the smaller the glitch area will be, and as the plot shows, when the multiple of the input FET size is 1, the buffer has the smallest glitch area.

4.3 5T Buffer

The strategy for improving the input range for the 5T and 7T buffer is the same as for the op-amps, which is reducing each FET's voltage headroom, so there will be more voltage range left for the signal swing. For the op-amp based buffers, their closed-loop gain is $A_{CL} = A_{OL}/(1 + A_{OL}\beta)$. The higher the open-loop gain A_{OL} is, the higher linearity is going to be, because as the A_{OL} is higher, its inverse is much lower, and the feedback network β takes more weight in the gain equation.

The AC test bench for testing the 5-T buffer is shown in Figure 40. The square box on the left is the circuit with the node of testing brought out and connected to the buffer. The AC small signal is connected to a DC decoupling capacitor and injecting a test voltage at the output of the buffer. The AC testing results are plotted in
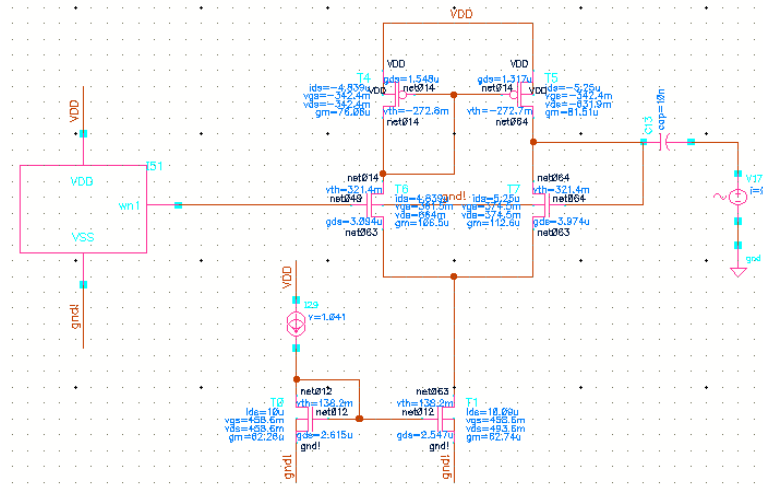
Figure 40 5T buffer backward gain AC test bench.
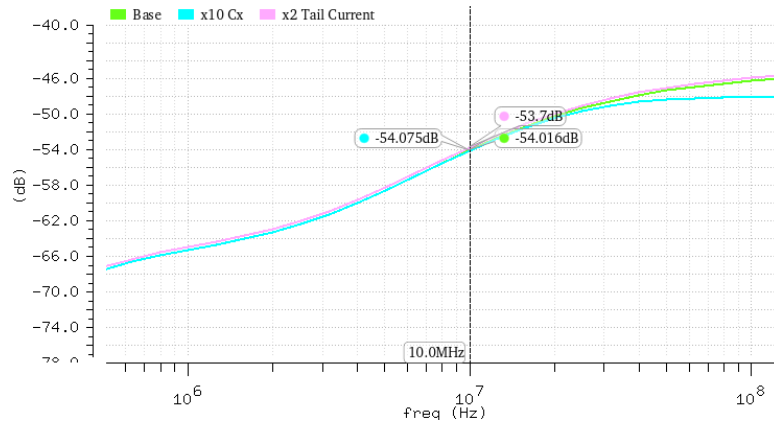
Figure 41 5T buffer backward gain optimization with AC simulation.

The isolation gets improved when a capacitor with the capacitance of 10 times bigger

than the C_X used to connect the node V_X to the gate of the tail current FET. And even though, the

AC performance became worse while increasing the tail current, but as it has shown in the

transient simulation below, the isolation is actually improved.
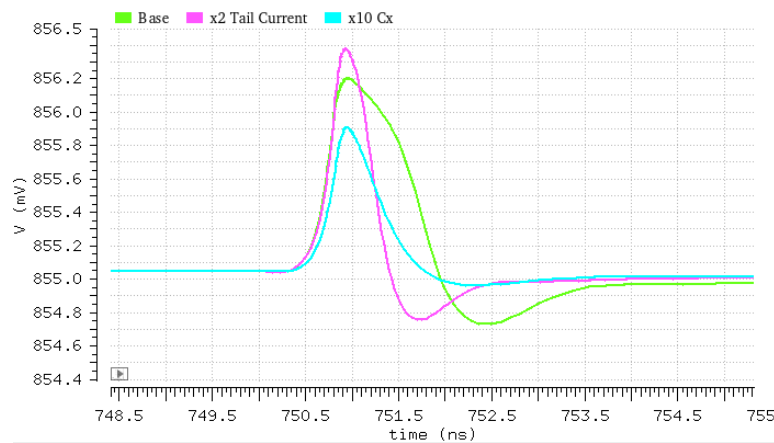
Figure 42 5T buffer backward gain optimization with transient simulation.

Looking at the transient plot, the reason that x2 Tail Current's isolation goes down in the

AC simulation is that the peak of the glitch initially went up and higher than the base version, but

it settles down to the steady-state much sooner than the base version. This explains the reason for

the worse AC performance because, in the AC simulation, the reverse gain is a voltage gain, so

as shown in the transient, when the peak goes higher, the AC reverse gain is bound to be worse.
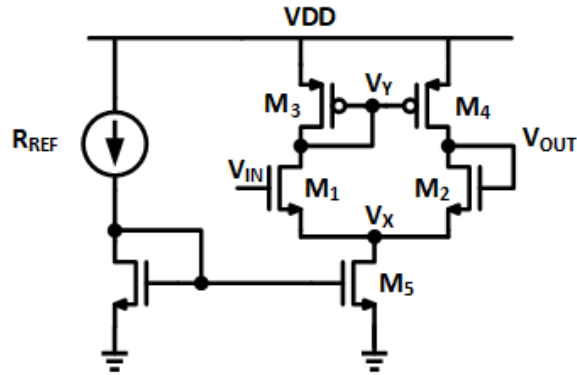
Figure 43 5T buffer schematic.

The reason that increasing the tail current can minimize the glitch is that more tail current means higher g_m value for the input pair, which means higher gain from V_{IN} to V_Y, and it makes M4 faster to shut off the current going into the M2 and to reduce the V_{OUT} faster. And from the transient plot we can see increasing the tail current is a better approach to reduce the glitch than increase the node capacitance, because it results in lower voltage peak and faster settling time.

4.4 7T Buffer

The two stages' tail currents in the 7T buffer are biased separately so that it can be investigated if each tail current will affect the overall isolation performance. The node of testing is the same as the previous one and the testing method is also the same.
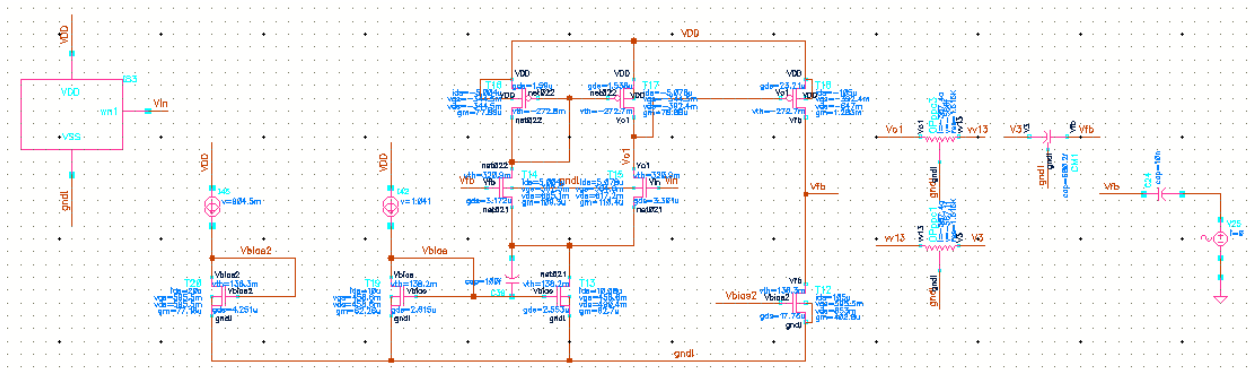
Figure 44 7T buffer AC test bench.
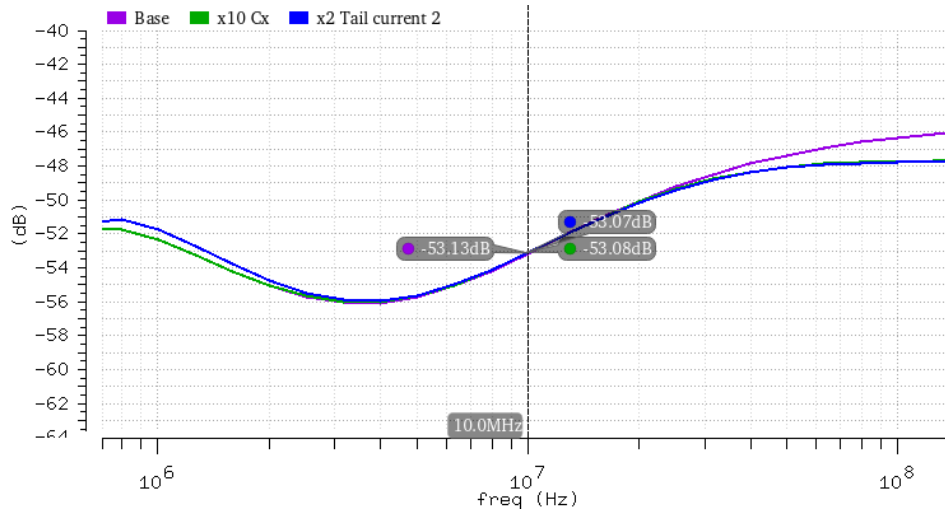
Figure 45 7T buffer backward gain AC performance.
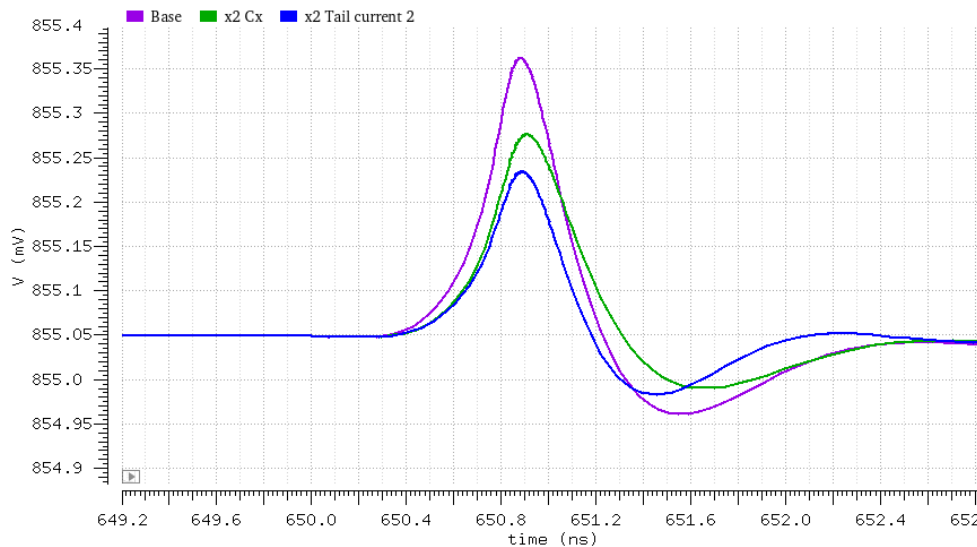
Figure 46 7T backward gain transient performance.

The AC performance of the 7-transistor buffer is shown in Figure 45. The shape of the transfer curve resembles a capacitor voltage divider followed by a high-pass filter. As the derived backward gain equation in Chapter 3, adding a capacitor in parallel with C_X or increasing the tail current can improve the backward gain. The improvement is not obvious in the AC plot, but very obvious in the transient plot. The reason for this difference is if we look at the voltage peak compare to the settled voltage in the transient plot, the maximum voltage difference is .3mV which is less than .035%, that is why the improvement is not obvious on the AC plot.

But overall, the glitch area has been reduced either by adding a capacitor or increasing the tail current.

4.5 Buffer Performance Summary

While designing all six buffers, the input FET's size is fixed to the same for all the buffers and the rest of the transistors are sized to be in the saturation region, and all buffers have the same amount of current. The reason for fixing the input FETs in the same size is because the backward gain of the buffers is related to the input FET size, so fixing the input FET's size can allow us to compare the rest of other specs, such as input range, forward gain, bandwidth and etc.

In Figure 47, the plot shows the inputs of all buffers are swept from 0 to 1.5V and plot the output voltage. As it's shown in the plot, 5T and 7T have the largest input range and follows the SSF. PSSF is good from 0 to 1.1V and NSSF is good for .4V to close to 1.5V. The most compressed are FVF, PFVF is good for .8V to 1V and NFVF is good for .4V to less than 1V. Since the buffers in this thesis are only used for connecting DC voltages, so input range is not a big concern, to get better input range for other applications, all the FETs need to be redesigned.
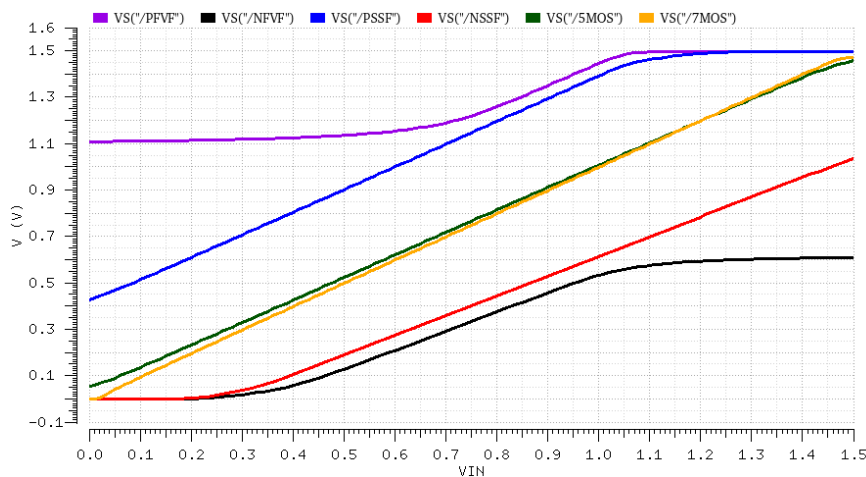
Figure 47 Input vs. output DC sweep for all buffers.

After taking the derivative for the plot in Figure 47, the plot in Figure 48 shows the Vin vs. Gain for all the buffers. There are two information can be read from this plot, the first is the

liner input range for buffers and second is how close these buffers are to 1 or 0dB. The linear

range is the range for which the gain of the buffer stays flat, and as it's shown from the plot

below, the result is as we got from Figure 47 that 7T and 5T have the best linear range, FVFs

have the worst linear range.
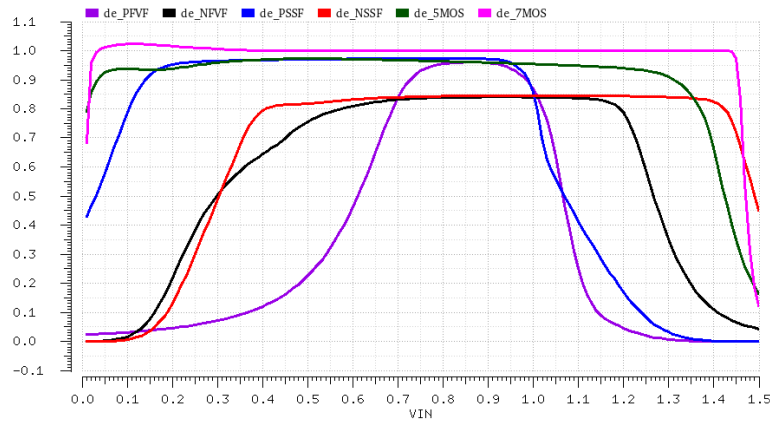
Figure 48 Vin vs. Vout derivative for all buffers.

The forward gain vs. frequency plot is shown in Figure 49, from the plot we can see 7-

transistor has the narrowest bandwidth and NFVF has the widest bandwidth, but 7T's gain is

much closer to 0 dB than NFVF's, so there's a trade-off between gain and bandwidth while

selecting which buffer topology to use. For the broadband applications, PFVF is a desirable

choice given it has a gain relatively close to 0dB and very wide bandwidth.
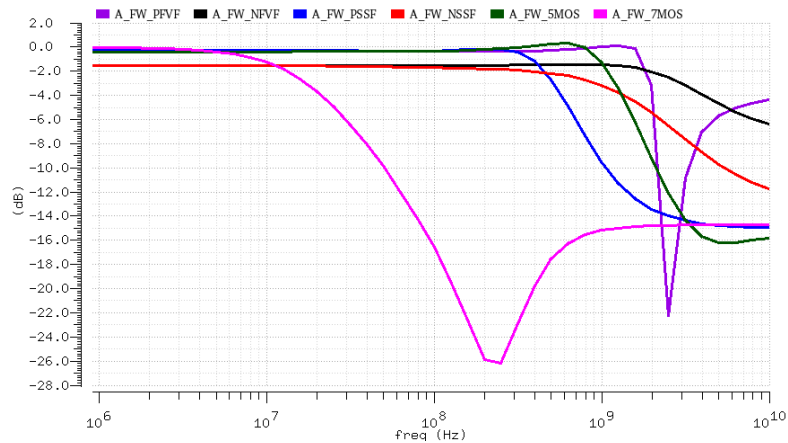
Figure 49 Forward gain frequency response for all buffers.

Output impedance for all the buffers is shown in Figure 50, as output impedance is an important spec we care about while using the buffer. From the plot we can see before around 0.5MHz, 7T has the lowest output impedance, followed by FVF and then the SSF and the 5T have the most output impedance, which is not ideal for applications like driving an LDO's power FET.
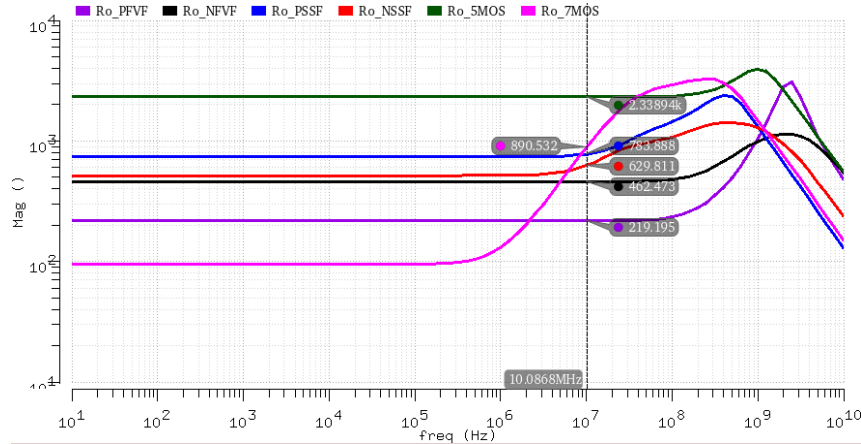
Figure 50 Output impedance vs. frequency for all buffers.

Figure 51 shows the reverse gain for all the buffers at 10MHz. As it can be seen from the plot, 5MOS and 7MOS have the best isolation performance, followed by PSSF and PFVF, and the least are NSSF and NFVF. Ideally, if the size of the input FET's is the same, P version and N version should have the same isolation, but in GF130nm process, with the same FET size, NMOS has slightly larger Cgs than PMOS, this explains why P version buffer has superior reverse gain than the N version.
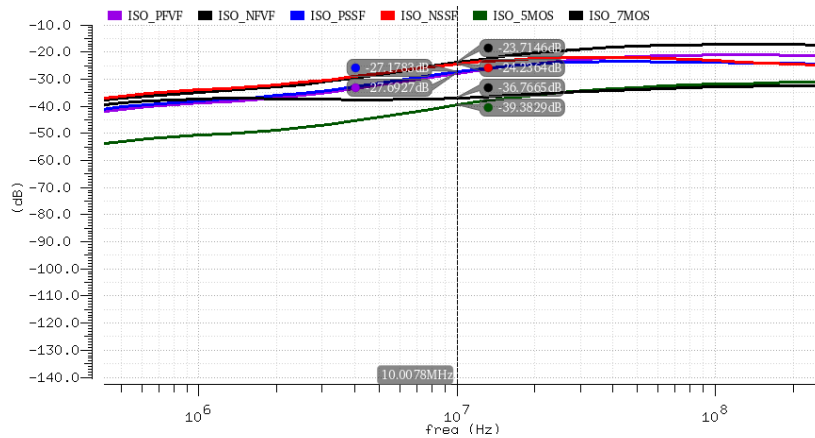
Figure 51 Buffer simulated backward gain vs. frequency.

As it was mentioned before that a buffer can be used for many applications, so to do a meaningful comparison of buffers between different topologies they need to be put into the context of specific applications. If the buffer is used to reduce the glitch noise, the backward gain will be the focus. In this case, if the area is not a big concern, the best options are 5T > 7T > PFVF > NFVF > PSSF > NSSF. If the area is considered, then PFVF > NFVF > 5T, others are excluded because the area is much larger than these three.

If the buffer is used for high accuracy applications, like the sample and hold the block in an Analog-to-Digital converter (ADC) [16], the accuracy and input range is the utmost concern, so the 7T will be the best fit up to the 7T's bandwidth. If the higher sampling rate is required, the PSSF or 5T will be the two good choices, and there is a trade-off between accuracy and bandwidth. The NSSF and FVF are excluded because NSSF's gain is off to 1 too much, and FVFs' input ranges are too narrow.

If the buffers are used in the LDO case, the output impedance, power, and area will be the main concerns. So, right of the bat, 7T and SSFs will be excluded, because their areas are too large; then the 5T is also not good, because its output impedance is large. So FVFs will be the good fits due to their small area and low output impedance.

Table 3 Buffer small-signal equation summary.

	Forward Gain A_V	Backward Gain A_{ISO}	Output Resistance R_o
SSF	$\dfrac{g_{m1}r_{o1}}{1 + (g_{m1})r_{o1} + \dfrac{1}{g_{m2}r_{02}}}$	$\dfrac{C_{gs1}}{C_{IN}}$	$\dfrac{1}{g_{m1}g_{m2}r_{01}}$
FVF	$\dfrac{g_{m1}}{g_{ds1} + g_{ds2} + g_{m1}}$	$\dfrac{C_{gs1}}{C_{IN}}$	$\dfrac{1}{g_{m1}g_{m2}r_{o1}}$
5T	$\dfrac{1}{1/A + 1}$, A$= \dfrac{g_{m1}}{g_{ds2} + g_{ds4}}$	$\dfrac{sC_{gs2} + g_{m2}}{sC_{gs2} + g_{m2} + sC_X + g_{ds5}} * \dfrac{sC_{gs1}}{1 + sC_{gs1}Z_S}$	$\dfrac{1}{g_{m2}}$
7T	$\dfrac{1}{1/A + 1}$, $A = \dfrac{g_{m1} * g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}$	$\dfrac{C_{gs1}}{C_{gs1} + C_X} * \dfrac{sC_{gs2}}{1 + sC_{gs2}Z_S}$	$\dfrac{1}{g_{m1}g_{m6}r_{o1}}$

Table 4 Simulated buffer performance summary.

	NSSF	PSSF	NFVF	PFVF	5T	7T
I_DC (uA)	35	35	35	35	35	35
Linearity (Number of Bits)	9.7	9.3	8.3	8.6	7.4	13.7
Forward Gain (dB)	-1.63	-0.3	-1.5	-0.34	-0.33	-0.05
Backward Gain (dB) at 10MHz	-24	-27	-24	-28	-39	-37
3dB Bandwidth w/ 10fF load cap	1.6 GHz	540 MHz	3.6 GHz	2 GHz	1.28 GHz	17 MHz
Output impedance (Ω)	630	780	460	220	2.3k	890
Input range (V)	0.61~1.4	0.2~0.95	0.68~1.2	0.75~0.9	0.5~1.3	0.4~1.4
ΔInput range (V)	0.79	0.75	0.52	0.15	0.8	1
Area (μm^2)	99	94	4.4	4.6	27	138.7

CHAPTER 5. CONCLUSION

In developing monitoring circuits, buffers can be used to decouple testing nodes from monitoring circuits, and also, they can be used to suppress glitches generated by monitoring circuits.

Chapter 1 not only provided literature reviews on monitoring-circuit topologies and their operating principles, but also provided reviews of analog buffers, described investigations on how they were used, and what parameters should be tested.

In chapter 2, topologies of six commonly used analog buffers were introduced, and their input range, small-signal forward gain, and output resistance were covered in this chapter.

Chapter 3 focused on small-signal reverse gain equations derivation. These equations are useful for sizing and biasing buffers to reduce the negative impact of using the monitoring circuits.

Chapter 4 described the design and simulation of six commonly used buffers, with the simulation results summarized in a table for the comparison purposes. The chapter concluded by describing buffer selection strategies for different applications based on the summarized table.

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APPENDIX BUFFER NUMBER OF BITS CALCULATION MATLAB CODE

```matlab
function [ dnl,inl ] = inl_inputV( V )
%Input V, and calculate INL
%Detailed explanation goes here
[M N]=size(V);
bw = diff(V);
dnl = (bw - mean(bw))/mean(bw);
dnl=dnl/N*1e6;
inl = [0 cumsum(dnl)];
end

%This script is used to calculate the linearity of the buffers
%function inl_inputV.m is used.
%For 5 and 7 mos buffer
X = VSVOUTX(10:62);
Y = VSVOUTY(10:62);
Y = Y.';
[dnl,inl] = inl_inputV(Y);
dnl_max = max(abs(dnl))
inl_max = max(abs(inl))   %Units for inl & dnl is ppm
NBits= log(10^6/inl_max)/log(2)
```